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CLAIMS

- A semiconductor structure comprising: 1.
- a monocrystalline oxide material; and
- a monocrystalline compound semiconductor material of first type formed overlying the monocrystalline oxide 10 material.
- The semiconductor structure of claim 1 further comprising a template layer formed between the monocrystalline oxide material and the monocrystalline compound semiconductor material of first type. 15
 - The semiconductor structure of claim 1 further comprising a buffer layer of monocrystalline semiconductor material of second type formed between the monocrystalline oxide material and the monocrystalline compound semiconductor material of first type.
- The semiconductor structure of claim 3 further comprising a template layer formed between the monocrystalline oxide material and the buffer layer of 25 monocrystalline semiconductor material of second type.
- The semiconductor structure of claim 3 wherein the buffer layer comprises a monocrystalline semiconductor material selected from the group consisting of: 30 Germanium, a GaAs_xP_{1-x} superlattice, an In_yGa_{1-y}P superlattice, and an InGaAs superlattice.



- 6. The semiconductor structure of claim 1 wherein the monocrystalline oxide material comprises an oxide selected from the group consisting of alkaline earth metal titanates, alkaline earth metal zirconates, alkaline earth metal hafnates, alkaline earth metal tantalates, alkaline earth metal ruthenates, alkaline earth metal niobates, alkaline earth metal vanadates, alkaline earth metal tin based perovskites, lanthanum aluminate, lanthanum scandium oxide and gadolinium oxide.
- 7. The semiconductor structure of claim 1 wherein the monocrystalline oxide material comprises $Sr_zBa_{1-z}TiO_3$ wherein z ranges from 0 to 1.
- 15 8. The semiconductor structure of claim 1 wherein the monocrystalline oxide material comprises a perovskite oxide.
- 9. The semiconductor structure of claim 1 wherein the
 20 monocrystalline compound semiconductor material comprises
 a material selected from the group consisting of: III-V
 compounds, mixed III-V compounds, II-VI compounds, and
 mixed II-VI compounds.
- 25 10. The semiconductor structure of claim 1 wherein the monocrystalline compound semiconductor material comprises a material selected from the group consisting of: GaAs, AlGaAs, InP, InGaAs, InGaP, ZnSe, AlInAs, CdS, CdHgTe, and ZnSeS.



11. A semiconductor structure comprising:

a monocrystalline oxide material having a first characteristic; and

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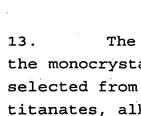
a monocrystalline compound semiconductor material having a second characteristic grown on the monocrystalline oxide material; and

wherein the first and second characteristics relate to each other in a manner selected from the group consisting of:

the first and second characteristics are lattice constants and the first and second characteristics are substantially matched; and

the first and second characteristics are related to crystal orientation of the monocrystalline oxide material and the monocrystalline compound semiconductor material and wherein the crystal orientations are rotated with respect to each other.

12. The semiconductor structure of claim 11 wherein the monocrystalline compound semiconductor material comprises a material selected from the group consisting of: GaAs, AlGaAs, InP, InGaAs, InGaP, ZnSe, and ZnSeS.



The semiconductor structure of claim 11 wherein the monocrystalline oxide material comprises an oxide selected from the group consisting of alkaline earth metal titanates, alkaline earth metal zirconates, alkaline earth metal hafnates, alkaline earth metal tantalates, alkaline earth metal ruthenates, alkaline earth metal niobates, alkaline earth metal vanadates, alkaline earth metal tin based perovskites, lanthanum aluminate, lanthanum scandium oxide and gadolinium oxide.

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- The semiconductor structure of claim 11 wherein 14. the monocrystalline oxide material comprises Sr₂Ba₁₋₂TiO₃ wherein z ranges from 0 to 1.
- The semiconductor structure of claim 11 wherein 15 15. the crystal orientations are rotated by 45 degrees with respect to each other.
 - A semiconductor structure comprising: 16.

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a monocrystalline semiconductor substrate;

an amorphous layer overlying the monocrystalline semiconductor substrate;

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- a monocrystalline oxide layer overlying the amorphous layer; and
- a monocrystalline compound semiconductor layer overlying the monocrystalline oxide layer. 30
 - The semiconductor structure of claim 16 wherein the monocrystalline semiconductor substrate comprises a layer of a material comprising silicon.



- 18. The semiconductor structure of claim 17 wherein the amorphous layer comprises a silicon oxide.
- 19. The semiconductor structure of claim 16 further
 5 comprising a template layer between the monocrystalline oxide layer and the monocrystalline compound semiconductor layer.
- 20. The semiconductor structure of claim 19 further comprising a buffer layer between the template layer and the monocrystalline compound semiconductor layer.
 - 21. The semiconductor structure of claim 16 further comprising a buffer layer between the monocrystalline oxide layer and the monocrystalline compound semiconductor layer.
- 22. The semiconductor structure of claim 21 wherein the buffer layer comprises a layer of semiconductor 20 material.
 - 23. The semiconductor structure of claim 16 wherein the monocrystalline oxide material comprises $Sr_zBa_{1-z}TiO_3$ wherein z ranges from 0 to 1.
 - 24. The semiconductor structure of claim 16 wherein the monocrystalline compound semiconductor material comprises a material selected from the group consisting of: GaAs, AlGaAs, InP, InGaAs, InGaP, ZnSe, and ZnSeS.



A semiconductor structure comprising:

a monocrystalline substrate characterized by a first lattice constant;

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a monocrystalline insulator layer having a second lattice constant different than the first lattice constant overlying the monocrystalline substrate; and

- a monocrystalline compound semiconductor layer having 10 a third lattice constant different than the first lattice constant overlying the monocrystalline insulator layer.
- The semiconductor structure of claim 25 wherein 15 the third lattice constant is different from the second lattice constant.
- The semiconductor structure of claim 25 further 27. comprising an amorphous oxide layer between the 20 monocrystalline substrate and the monocrystalline . insulator layer.
- The semiconductor structure of claim 27 wherein 28. the amorphous oxide layer has a thickness sufficient to 25 relieve strain in the monocrystalline insulator layer.
- The semiconductor structure of claim 25 further 29. comprising a template layer between the monocrystalline insulator layer and the monocrystalline compound 30 semiconductor layer.

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- The semiconductor structure of claim 25 further comprising a buffer layer between the monocrystalline insulator layer and the monocrystalline compound semiconductor layer.
- 31. The semiconductor structure of claim 25 wherein the monocrystalline substrate is characterized by a first crystalline orientation and the monocrystalline insulator layer is characterized by a second crystalline orientation and wherein the second crystalline orientation is rotated with respect to the first crystalline orientation.
- 32. The semiconductor structure of claim 25 wherein the monocrystalline substrate comprises silicon.
- The semiconductor structure of claim 25 wherein the monocrystalline substrate comprises a material comprising silicon, the monocrystalline insulator comprises an alkaline earth metal titanate and the monocrystalline compound semiconductor material comprises a material selected from the group consisting of: GaAs, AlGaAs, ZnSe, and ZnSeS.
- 34. The semiconductor structure of claim 33 wherein the monocrystalline insulator layer comprises $Sr_zBa_{1-z}TiO_3$ where z ranges from 0 to 1.
- 35. The semiconductor structure of claim 25 wherein the monocrystalline insulator comprises an oxide selected 30 from the group consisting of alkaline earth metal zirconates, and alkaline earth metal hafnates and the monocrystalline compound semiconductor layer comprises a material selected from the group consisting of: InP and InGaP.



a monocrystalline substrate characterized by a first lattice constant;

- a monocrystalline nitride layer having a second lattice constant different than the first lattice constant overlying the monocrystalline substrate; and
- a monocrystalline compound semiconductor layer having a third lattice constant different than the first and second lattice constants overlying the monocrystalline nitride layer.
- 15 37. The semiconductor structure of claim 36 wherein the monocrystalline nitride comprises a material selected from the group consisting of gallium nitride, aluminum nitride and boron nitride.

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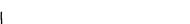
a first monocrystalline semiconductor substrate comprising silicon and having a first region and a second region;

an intermediate layer comprising a silicon oxide overlying the first region;

- a first monocrystalline oxide layer overlying the intermediate layer;
 - a second monocrystalline semiconductor layer overlying the first monocrystalline oxide layer;
 - a second monocrystalline oxide layer overlying the second monocrystalline semiconductor layer; and
- a third monocrystalline semiconductor layer overlying
 the second monocrystalline oxide layer and wherein at
 least one of the second monocrystalline semiconductor
 layer and the third semiconductor layer comprises a
 compound semiconductor material.
- 25 39. The semiconductor structure of claim 38 further comprising a template layer between the first monocrystalline oxide layer and the second monocrystalline semiconductor layer.
- 30 40. The semiconductor structure of claim 38 further comprising an active semiconductor component positioned at least partially in the second region.

- 41. The semiconductor structure of claim 40 further comprising a second semiconductor component positioned at least partially in the second monocrystalline semiconductor layer.
- 42. The semiconductor structure of claim 41 wherein the second monocrystalline oxide layer comprises a gate dielectric of the second semiconductor component.
- 10 43. The semiconductor structure of claim 41 further comprising an electrical interconnection between the active semiconductor component and the second semiconductor component.
 - 15 44. The semiconductor structure of claim 41 wherein the second monocrystalline semiconductor layer comprises a group III-V compound and the second semiconductor component comprises a component in a radio frequency amplifier.





45. A semiconductor device comprising:

a first monocrystalline semiconductor layer comprising a first region and a second region;

an electrical semiconductor component positioned at least partially within the first region;

a second monocrystalline compound semiconductor layer 10 overlying the second region; and

a second semiconductor component positioned at least partially within the second monocrystalline compound semiconductor layer.

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The semiconductor device of claim 45 further comprising a monocrystalline oxide layer positioned between the first region and the second monocrystalline compound semiconductor region.

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The semiconductor device of claim 46 further comprising an electrical interconnection between the active semiconductor component and the second semiconductor component.

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The semiconductor device of claim 46 wherein the first monocrystalline semiconductor layer comprises silicon and the monocrystalline oxide layer comprises a material selected from the group consisting of: alkaline earth metal titanates, alkaline earth metal zirconates, and alkaline earth metal hafnates.





49. The semiconductor device of claim 45 further comprising an electrical interconnection between the active semiconductor component and the second semiconductor component.

50. A process for fabricating a semiconductor structure comprising the steps of:

providing a monocrystalline semiconductor substrate comprising silicon;

epitaxially growing a monocrystalline oxide layer overlying the monocrystalline substrate;

- oxidizing the monocrystalline semiconductor substrate during the step of epitaxially growing to form a silicon oxide layer between the monocrystalline semiconductor substrate and the monocrystalline oxide layer;
- epitaxially growing a monocrystalline compound semiconductor layer overlying the monocrystalline oxide layer.
- 51. The process of claim 50 further comprising the 20 step of forming a first template layer on the monocrystalline semiconductor substrate.
- 52. The process of claim 51 wherein the step of providing a monocrystalline semiconductor substrate

 25 comprises providing a substrate having a silicon oxide layer on a surface thereof and the step of forming a first template layer comprises the steps of:
- depositing a material selected from the group

 30 consisting of barium and strontium onto the silicon oxide layer and

heating the substrate to react the material with the silicon oxide.

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53. The process of claim 51 wherein the step of providing a monocrystalline semiconductor substrate comprises providing a substrate having a silicon oxide layer on a surface thereof and the step of forming a first template layer comprises the steps of:

depositing strontium and oxygen onto the silicon oxide layer and

- 10 heating the substrate to react the strontium and oxygen with the silicon oxide.
 - 54. The process of claim 50 wherein the step of epitaxially growing a monocrystalline oxide layer comprises the steps of:

heating the substrate to a temperature between about 400°C and about 600°C; and

- introducing reactants comprising strontium, titanium, and oxygen.
- 55. The process of claim 54 wherein the step of introducing comprises controlling the ratio of strontium to titanium and controlling partial pressure of oxygen.
 - 56. The process of claim 55 wherein the step of oxidizing the monocrystalline semiconductor substrate comprises increasing the partial pressure of oxygen above a level necessary for epitaxially growing the monocrystalline oxide layer.
- 57. The process of claim 50 further comprising the step of forming a second template layer overlying the monocrystalline oxide layer.

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- 58. The process of claim 57 wherein the step of forming a second template layer comprises the step of capping the monocrystalline oxide layer with a layer comprising a monolayer of a material selected from the group consisting of titanium, titanium and oxygen, strontium, and strontium and oxygen.
- 59. The process of claim 58 wherein the step of epitaxially growing a monocrystalline compound semiconductor layer comprises:

depositing arsenic on the second template layer; and

- reacting the arsenic with the material of the second template layer.
 - 60. The process of claim 59 wherein the step of epitaxially growing a monocrystalline compound semiconductor layer further comprises the steps of deposing gallium and arsenic after the step of reacting.
- 61. The process of claim 57 further comprising the step of forming a buffer layer overlying the second 25 template layer.
 - 62. The process of claim 50 further comprising the step of forming a buffer layer overlying the monocrystalline oxide layer.
 - 63. The process of claim 62 wherein the process of forming a buffer layer comprises the step of epitaxially depositing a layer of germanium overlying the monocrystalline oxide layer.

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64. The process of claim 62 wherein the process of forming a buffer layer comprises the step of depositing a superlattice comprising a III-V group compound semiconductor material.

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65. The process of claim 50 wherein the step of epitaxially growing a monocrystalline oxide layer comprises the step of epitaxially growing an alkaline earth metal titanate.

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- 66. The process of claim 65 wherein the step of epitaxially growing a monocrystalline compound semiconductor layer comprises the step of epitaxially growing a layer from the group consisting of the GaAs, AlGaAs, ZnSe, and ZnSSe.
- 67. The process of claim 50 wherein the step of epitaxially growing a monocrystalline oxide layer comprises the step of epitaxially growing an oxide from the group consisting of the alkaline earth metal zirconates and the alkaline earth metal hafnates.
- 68. The process of claim 67 wherein the step of epitaxially growing a monocrystalline compound
 25 semiconductor layer comprises the step of epitaxially growing a monocrystalline layer of compound semiconductor material selected from the group consisting of InP and InGaAs.

- The process of claim 68 further comprising the step of forming a second template layer overlying the monocrystalline oxide layer by depositing a layer having a thickness of about 1-10 monolayers of a material selected from the group consisting of Zr-As, Zr-P, Hf-As, Hf-P, Sr-O-As, Sr-O-P, Sr-As, Sr-P, Ba-O-As, Ba-O-P, Ba-As, Sr-Ga-O, Ba-Ga-O, and Ba-P.
- 70. The process of claim 50 wherein the step of epitaxially growing a monocrystalline oxide layer comprises epitaxially growing at a growth rate of about 0.3-0.5 nm per minute.

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A process for fabricating a semiconductor structure comprising the steps of:

providing a monocrystalline semiconductor substrate;

epitaxially growing a monocrystalline oxide layer overlying the monocrystalline substrate;

oxidizing the monocrystalline semiconductor substrate during the step of epitaxially growing to form a silicon oxide layer between the monocrystalline semiconductor substrate and the monocrystalline oxide layer;

epitaxially growing a monocrystalline compound semiconductor layer overlying the monocrystalline oxide 15 layer.

72. A process for fabricating a semiconductor structure comprising the steps of:

providing a monocrystalline oxide layer having a 5 surface;

forming a template layer on the surface; and

epitaxially growing a monocrystalline compound 10 semiconductor layer overlying the template.

- 73. The process of claim 72 wherein the step of providing a monocrystalline oxide layer comprises providing a monocrystalline oxide layer comprising a material selected from the group consisting of alkaline earth metal titanates, alkaline earth metal zirconates, and alkaline earth metal hafnates.
- 74. The process of claim 72 wherein the step of
 20 providing a monocrystalline oxide layer comprises
 epitaxially growing a monocrystalline oxide layer lattice
 matched to an underlying monocrystalline silicon
 substrate.
- 75. The process of claim 72 wherein the step of providing a monocrystalline oxide layer comprises providing an oxide layer comprising Sr_zBa_{1-z}TiO₃ where z ranges from 0 to 1.
- The process of claim 75 wherein the step of forming a template layer comprises capping the oxide layer with 1-10 monolayers of a material selected from Ti, TiO, Sr, and SrO.

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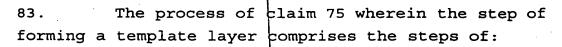
- 77. The process of claim 76 wherein the step of epitaxially growing a monocrystalline compound semiconductor layer comprises epitaxially depositing a layer selected from GaAs, AlGaAs, GaAsP, and GaInP.
- 78. The process of claim 76 further comprises the step of depositing a buffer layer overlying the template layer.
- 10 79. The process of claim 78 wherein the step of depositing a buffer layer comprises epitaxially depositing a superlattice layer of a material selected from GaAs_xP_{1-x} where x ranges from 0 to 1 and In_yGa_{1-y} P where y ranges from 0 to 1.
 - 80. The process of claim 79 wherein the step of epitaxially growing a monocrystalline compound semiconductor layer comprises epitaxially depositing a layer selected from GaAs, AlGaAs, GaAsP, GaInAs, InP and GaInP.
- 81. The process of claim 75 wherein the step of forming a template layer comprises capping the monocrystalline oxide layer with 1-10 monolayers of a material selected from Ge-Sr and Ge-Ti.
 - 82. The process of claim 81 further comprising the step of epitaxially depositing a buffer layer of germanium.

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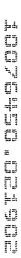
capping the monocrystalline oxide layer with 1-10 monolayers of ZnO; and

depositing 1-3 monolayers of zinc rich ZnO overlying the monolayers of ZnO.

- 10 84. The process of claim 83 wherein the step of epitaxially growing a monocrystalline compound semiconductor layer comprises epitaxially growing a layer selected from ZnSe and ZnSeS.
- 15 85. The process of claim 75 wherein the step of forming a template layer comprises the step of capping the monocrystalline oxide layer with 1/-2 monolayers of SrS.
- 86. The process of claim 85 wherein the step of
 20 epitaxially growing a monocrystalline compound
 semiconductor layer comprises epitaxially growing a layer
 of ZnSeS.
- 87. The process of claim 72 wherein the step of providing a monocrystalline oxide layer comprises providing a monocrystalline oxide layer comprising a material selected from the group consisting of alkaline earth metal zirconates, and alkaline earth metal hafnates.
- 30 88. The process of claim 87 wherein the process of forming a template layer comprises capping the monocrystalline oxide layer with 1-10 monolayers of a material selected from Zr-As, Zr-P, Hf-As, Hf-P, Sr-As, Sr-O-As, Sr-P, Sr-O-P, Ba-As, Ba-O-As, Ba-P, Sr-Ga-O, 35 Ba-Ga-O, and Ba-O-P.









- 89. The process of claim 88 wherein the step of epitaxially growing a monocrystalline compound semiconductor layer comprises epitaxially growing a layer comprising a material selected from InP and InGaAs.
- 90. The process of claim 89 further comprising a buffer layer comprising a superlattice comprising InGaAs where indium ranges from 0 to about 47% deposited overlying the template.

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A process for fabricating a semiconductor structure comprising the steps of:

providing a monocrystalline semiconductor substrate;

forming an accommodating buffer layer overlying the monocrystalline semiconductor substrate;

forming an amorphous intermediate layer between the monocrystalline semiconductor substrate and the 10 accommodating buffer layer; and

epitaxially growing a monocrystalline compound semiconductor layer overlying the accommodating buffer layer.

- 92. The process of claim 91 wherein the step of forming an amorphous intermediate layer comprises the step of diffusing oxygen through the accommodating buffer layer to oxidize the monocrystalline semiconductor substrate. 20
- The process of claim 91 wherein the step of forming an accommodating buffer layer comprises growing an epitaxial layer by a process selected from MBE, MOCVD, 25 MEE, and ALE.
- The process of claim 91 wherein the step of providing a monocrystalline semiconductor substrate comprises providing a monocrystalline silicon substrate having a silicon oxide layer on a surface thereof. 30



- 95. The process of claim 94 wherein the step of forming an accommodating buffer layer comprises the steps of:
- reacting a material selected from Sr and SrO with the silicon oxide layer to form a template on the silicon substrate surface; and
- epitaxially deposing a layer comprising Sr_zBa_{1-z}TiO₃

 10 wherein z ranges from 0 to 1 on the template.
 - 96. The process of claim 91 further comprising the step of forming a template overlying the accommodating buffer layer prior to the step of epitaxially growing.

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97. A process for fabricating a semiconductor structure comprising the steps of:

providing a monocrystalline silicon substrate

comprising a first region and a second region, the second region having an oxidized surface;

forming a CMOS circuit in the first region;

depositing a material comprising strontium onto the second region having an oxidized surface and reacting the material with the oxidized surface to form a first template layer;

depositing a monocrystalline oxide layer comprising strontium, titanium and oxygen overlying the first template layer by introducing strontium, titanium, and a partial pressure of oxygen to the template layer;

increasing the partial pressure of oxygen to grow an amorphous layer of silicon oxide on the second region;

terminating the step of depositing a monocrystalline oxide layer by depositing a second template layer comprising a monolayer comprising titanium;

depositing a layer of a monocrystalline compound semiconductor material comprising gallium and arsenic overlying the second template layer;

forming a semiconductor component in the layer of a monocrystalline compound semiconductor material; and

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depositing a metallic conductor configured to electrically couple the CMOS circuit and the semiconductor component.

- 5 98. A semiconductor structure comprising:
 - a monocrystalline semiconductor substrate;
- a monocrystalline oxide layer comprising Sr_zBa_{1-z}TiO₃

 10 overlying the monocrystalline semiconductor substrate,
 wherein z ranges from 0 to 1; and

an amorphous layer positioned between the monocrystalline semiconductor substrate and the monocrystalline oxide layer.

- 99. The semiconductor structure of claim 89 wherein the monocrystalline semiconductor substrate comprises a Group IV element.
- 100. The semiconductor structure of claim 98 wherein the monocrystalline oxide layer has a thickness greater than 20 nm.
- 25 101. The semiconductor structure of claim 98 wherein the amorphous layer comprises silicon oxide and has a thickness sufficient to relieve strain in the monocrystalline oxide layer.
- 30 102. The semiconductor structure of claim 98 wherein the amorphous layer comprises silicon oxide and has a thickness greater than 1.0 nm.

103. The semiconductor structure of claim 98 wherein the amorphous layer comprises silicon oxide and has a thickness of 0.5 20 2.5 nm.

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- 104. A communicating device including an integrated circuit, wherein the integrated circuit comprises: an accommodating buffer layer;
 - a compound semiconductor portion overlying the accommodating buffer layer, wherein the compound semiconductor portion includes a feature selected from a group consisting of an amplifier, a modulating circuit, and a demodulating circuit; and
- a Group IV semiconductor portion including a digital logic portion coupled to the feature.
- 105. The communicating device of claim 104, wherein the compound semiconductor portion has a crystal orientation that is rotated by approximately 45° with respect to a crystal orientation of the accommodating buffer layer.
- 20 106. The communicating device of claim 105, wherein:
 the integrated circuit further comprises a
 monocrystalline Group IV substrate underlying the
 compound semiconductor portion; and
 the accommodating buffer layer has a crystal
 orientation that is rotated by approximately 45°
 with respect to a crystal orientation of the
 monocrystalline Group IV substrate.
- 107. The communicating device of claim 106, wherein the
 accommodating buffer layer and the compound semiconductor portion have greater than approximately 2.0% and a thickness of the compound semiconductor portion is at least approximately 20 nm.

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The communicating devide of claim 104, wherein the integrated circuit has a feature selected from a group consisting of: 5 the accommodating buffer layer has a crystal orientation that is rotated by approximately 45° with respect to a crystal orientation of the compound semiconductor portion; and the accommodating buffer layer and the compound semiconductor portion have a lattice mismatch no 10 greater than approximately 2.0% and a thickness of the compound semiconductor portion is at least approximately 20 nm. The communicating device of claim 104, wherein the

15 integrated circuit further comprises a monocrystalline Group IV substrate underlying the monocrystalline compound semiconductor portion, wherein: the accommodating buffer layer has a crystal 20 orientation that is rotated by approximately 45° with respect to a crystal orientation of the monocrystalline Group IV substrate; and the accommodating buffer layer and the compound semiconductor portion have a lattice mismatch no greater than approximately 2.0% and a thickness of 25 the compound semiconductor portion is at least approximately 20 nm.

The communicating device of claim 104, wherein the accommodating buffer layer and the compound semiconductor portion have a lattice mismatch no greater than approximately 2.0% and a thickness of the compound semiconductor portion is at least approximately 20 nm.

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111.	A communicating device including
	a signal transceiving means;
	an integrated circuit including:

- a compound semiconductor portion having an amplifier coupled to the signal transceiving means:
- a Group IV semiconductor portion having a digital signal processing means coupled to the amplifier; and a unit coupled to the integrated circuit.
- 112. The communicating device of claim 111, wherein the communicating device includes a portable telephone.
 - 113. The communicating device of claim 111, wherein the communicating device is a cellular telephone.
- 20 114. The communicating device of claim 111, wherein the Group IV semiconductor portion includes a converter selected from a group selected from a digital-to-analog converter and an analog-to-digital converter, wherein the converter is coupled to the unit.
 - 115. The communicating device of claim 111, wherein the unit is selected from a group consisting of keyboard, a microphone, a speaker, a visual display, and a memory means.

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- 116. The communicating device of claim 111, wherein:
 the Group IV semiconductor portion includes a bipolar
 portion and a field effect portion; and
 the bipolar portion includes a signal modulating
 means coupled to the digital signal processing
 means and the amplifier.
- 117. The communicating device of claim 111, wherein the compound semiconductor portion further includes a signal modulating means.
- 118. The communicating device of claim 111, wherein: the signal transceiving means includes an antenna; the amplifier is a Group III-V semiconductor power amplifier;
 - the integrated circuit includes a bipolar portion having a radio frequency to intermediate frequency mixer coupled to the Group III-V semiconductor power amplifier and the digital signal processing means;

the unit includes a microphone; and the communicating device further includes a speaker.

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- 119. An integrated circuit comprising:
 - a monocrystalline Group IV semiconductor substrate;
 - a compound semiconductor portion including a laser overlying the monocrystalline Group IV semiconductor substrate; and
 - a Group IV semiconductor portion including an electrical component coupled to the laser, wherein the Group IV semiconductor portion lies within or over the monocrystalline Group IV semiconductor substrate.
- 120. The integrated circuit of claim 119, further comprising a waveguide, wherein the waveguide is coupled to the laser and to the electrical component.
- 121. The integrated circuit of claim 119, wherein the electrical component is a transistor.
- 122. The integrated circuit of claim 119, wherein the Group IV semiconductor portion includes CMOS transistors, of which, the electrical component is one of the CMOS transistors.
- 123. The integrated circuit of claim 119, further

 comprising an accommodating buffer layer lying between the monocrystalline Group IV semiconductor substrate and the compound semiconductor portion.
- 124. The integrated circuit of claim 123, further

 comprising a waveguide, wherein the waveguide is coupled to the laser and the electrical component, and wherein the waveguide comprises at least a portion of the accommodating buffer layer.



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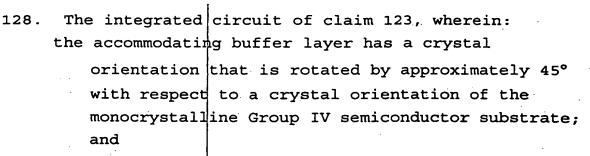
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- 125. The integrated circuit of claim 123, wherein the compound semiconductor portion has a crystal orientation that is rotated by approximately 45° with respect to a crystal orientation of the accommodating buffer layer.
- 126. The integrated circuit of claim 125, wherein the accommodating buffer layer has a crystal orientation that is rotated by approximately 45° with respect to a crystal orientation of the monocrystalline Group IV semiconductor substrate.
- 127. The integrated circuit of claim 123, wherein the integrated circuit has a feature selected from a group consisting of:
 - the accommodating buffer layer has a crystal orientation that is rotated by approximately 45° with respect to a crystal orientation of the monocrystalline Group IV semiconductor substrate; and
 - the accommodating buffer layer and the compound semiconductor portion have a lattice mismatch no greater than approximately 2.0% and a thickness of the compound semiconductor portion is at least approximately 20 nm.

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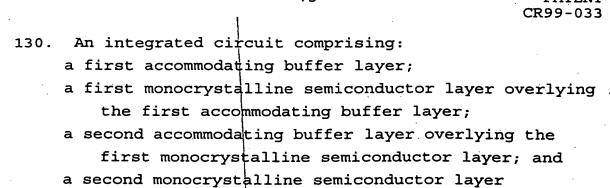
the accommodating buffer layer and the compound semiconductor portion have a lattice mismatch no greater than approximately 2.0% and a thickness of the compound semiconductor portion is at least approximately 20 nm.

129. The integrated circuit of claim 123, wherein the accommodating buffer layer and the compound semiconductor portion have a lattice mismatch no greater than approximately 2.0% and a thickness of the compound semiconductor portion is at least approximately 20 nm.

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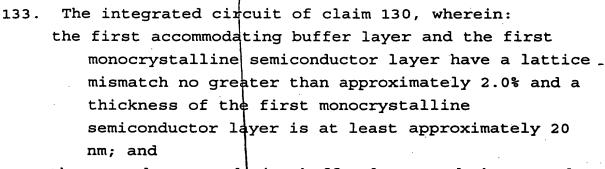
- 131. The integrated circuit of claim 130, wherein: 10 one of the first and second monocrystalline semiconductor layers is a monocrystalline compound semiconductor layer; and
 - the other of the first and second monocrystalline semiconductor layers is a monocrystalline Group IV semiconductor layer.

overlying the second accommodating buffer layer.

- The integrated circuit of claim 130, wherein: 132. the first monocrystalline semiconductor layer has a crystal orientation that is rotated by approximately 45° with respect to a crystal orientation of the first accommodating buffer layer;
 - the second accommodating buffer layer has a crystal orientation that is rotated by approximately 45° with respect to a crystal orientation of the first monocrystalline semiconductor layer; and

the second monocrystalline semiconductor layer has a

crystal orientation that is rotated by approximately 45° with respect to a crystal 30 orientation of the second accommodating buffer layer.



the second accommodating buffer layer and the second monocrystalline semiconductor layer have a lattice mismatch no greater than approximately 2.0% and a thickness of the second monocrystalline semiconductor layer is at least approximately 20 nm.

15 134. The integrated circuit of claim 130, further comprising a monocrystalline Group IV substrate underlying the first accommodating buffer layer.

an accommodating buffer layer; and active devices, wherein all the active devices lie at least partially within or over a monocrystalline compound semiconductor layer that overlies the accommodating buffer layer.

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136. The integrated circuit of claim 135, wherein: the integrated circuit includes electronic components;

the electronic components include the active devices active and at least one other component; and

all the electronic components lie at least partially within or over a monocrystalline compound semiconductor layer that overlies the accommodating buffer layer.

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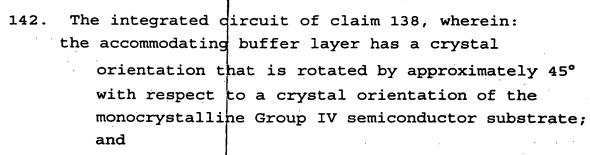
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- 137. The integrated circuit of claim 135, wherein the compound semiconductor layer has a crystal orientation that is rotated by approximately 45° with respect to a crystal orientation of the accommodating buffer layer.
- 138. The integrated circuit of claim 135, further comprising a monocrystalline Group IV semiconductor substrate that underlies the accommodating buffer layer.
- 139. The integrated circuit of claim 138, wherein the monocrystalline Group IV semiconductor substrate that is at least approximately 300 millimeters wide.
- 15 140. The integrated circuit of claim 138, wherein the accommodating buffer layer has a crystal orientation that is rotated by approximately 45° with respect to a crystal orientation of the monocrystalline Group IV semiconductor substrate.
 - 141. The integrated circuit of claim 138, wherein the integrated circuit has a feature selected from a group consisting of:
 - the accommodating buffer layer has a crystal orientation that is rotated by approximately 45° with respect to a crystal orientation of the monocrystalline Group IV semiconductor substrate; and
- the accommodating buffer layer and the

 monocrystalline Group IV semiconductor substrate
 have a lattice mismatch no greater than
 approximately 2.0% and a thickness of the
 accommodating buffer layer is at least
 approximately 20 mm.

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the accommodating buffer layer and the monocrystalline Group IV semiconductor substrate have a lattice mismatch no greater than approximately 2.0% and a thickness of the accommodating buffer layer is at least approximately 20 nm.

15 143. The integrated circuit of claim 135, wherein the accommodating buffer layer and the monocrystalline compound semiconductor layer have a lattice mismatch no greater than approximately 2.0% and a thickness of the monocrystalline compound semiconductor layer is at least approximately 20 nm.

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